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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/164,216	09/30/1998	RONALD PASQUALINI	NSC1-D8400	6392

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/164,216	PASQUALINI, RONALD	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15,19 and 38-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *40-44,67 and 68* is/are allowed.

6)☒ Claim(s) *15,19,38,39,45-57,60-62,65,66 and 69-72* is/are rejected.

7)☒ Claim(s) *58,59,63 and 64* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 15, 19, 38-39, 45-57, 60-62, 65-66 and 69-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al. (5,515,225) considered alone, or over Gens et al. in view of Admitted Prior Art (APA).

Gens et al. teach in figure 3 and related text a semiconductor chip having a substrate (figure 4, the external line encircling R1) of a first conductivity type, the chip comprising a plurality of pads P1, P2, an ESD negative ring R2, a plurality of ESD positive lines (the horizontal lines located between the high power supply terminals (the square blocks indicated as VDD1 and VDD2) and the line connecting the two diodes. See also column 3, lines 32-49), not being electrically connected to each other, not being directly connected to said pads, and not encircling the periphery of the chip; a plurality of switches (diodes) connected to the ESD positive lines and the ESD negative ring, and a plurality of first and second diodes D2, D1 connected to a pad and the negative ring and positive line, respectively.

Although Gens et al. do not explicitly state that plurality of switches are connected between the ESD positive lines and the ESD negative ring, this

feature is inherent in Gens et al.'s device, because it is well known in the art that diodes are switches, of which official notice is taken. Therefore, Gens et al. teach plurality of switches being connected between the ESD positive lines and the ESD negative ring, as claimed.

In the alternative, APA teaches in figures 1 and 2 and related text a plurality of ESD switches including a transistor (figure 2) connected to the positive line and to the negative ring, respectively (page 2, lines 24-27), wherein the transistor pass current from a positive line to a negative ring when a voltage on the positive line rises at a first rate. It would also have been obvious to a person of ordinary skill in the art at the time the invention was made to connect plurality of switches between the ESD positive lines and the ESD negative ring in Gens et al.'s device in order to provide more effective unidirectional flow of current during ESD operation.

The embodiment of figure 3 depicts a plurality of ESD positive lines being directly connected to VDD pads. That is, Gen et al. do not teach a plurality of ESD positive lines not being directly connected to VDD pads. Gen et al. teach that an artisan can modify the device by connecting a pair of parallel head to tail diodes between each high voltage supply (VDD) and the bus (R1) (column 4, lines 28-36). It would also have been obvious to a person of ordinary skill in the art at the time the invention was made to connect a pair of parallel head to tail diodes between each high voltage supply (VDD) and the bus (R1), adjacent to the high voltage supply (VDD), in Gens et al.'s device, so that the plurality of ESD positive

lines are not directly connected to the VDD pads, in order to improve the isolation between the various power supply sources.

Regarding claim 19, Gens et al. teach in figure 4 a negative line encircling the periphery of the chip.

Regarding claim 39, APA teaches in figure 2 a plurality of ESD switches including a transistor. It would also have been obvious to a person of ordinary skill in the art at the time the invention was made to use a transistor as an ESD switch in Gens et al.'s device, because it is well known in the art to use a transistor as an ESD switch in order to provide better switching capabilities.

Regarding claim 45, Gens et al. teach a plurality of ESD positive lines not being directly connected to a steady voltage source,

Regarding claim 46, Gens et al. teach in figure 3 a second diode having an anode electrically connected to a pad.

Regarding claims 51 and 62, APA teaches in figures 1 and 2 and related text a plurality of ESD switches including a transistor (figure 2) connected to the positive line and to the negative ring, respectively (page 2, lines 24-27), wherein the transistor pass current from a positive line to a negative ring when a voltage on the positive line rises at a first rate. It would also have been obvious to a

person of ordinary skill in the art at the time the invention was made to use a transistor as an ESD switch in Gens et al.'s device, in order to improve the switching capabilities of the device during an ESD event.

Regarding claim 52, Gens et al. teach in figure 3 switches (diodes) blocking a current from flowing from the positive line to the negative ring when a voltage on the positive line rises at a second rate that is different from the first rate.

Regarding claim 53, Gens et al. teach in figure 3 second diodes forward biased when the voltage on the positive line rises at a second rate.

Regarding claims 54, 61 and 66, Gens et al. teach in figures 3 and 4 that none of the positive lines encircles the periphery of the chip.

Regarding claim 55, Gens et al. teach in figure 3 a positive line connected to a negative ring via a plurality of ESD switches.

Regarding claims 56, 60 and 65, Gens et al. teach in figure 3 an ESD switch Z (figure 2, the right most diode) being directly connected to a positive and negative lines.

Regarding claim 57, Gens et al. teach in figure 3 that none of the positive lines being directly connected to a pad.

Regarding claims 57 and 62, Gens et al. teach in figure 3 only one second diode D1 is connected between a pad P2 and a positive line Vddi. Note that R1 is Vddi, a positive line (column 4, lines 7-8).

Regarding claim 62, Gens et al. teach in figure 3 a plurality of ESD switches D1, Z connected to the ESD positive lines and ESD negative ring so that each switch connected to a positive line and the ESD negative ring, and a switch Z of the plurality of ESD switches passing a current from the positive line to the negative ring when a voltage on the positive line rises at a first rate that is faster than a second rate.

Regarding claims 69-72, Gens et al. teach in figure 3 a second diode D1 (the diode connected between pad P1 and R1) being directly connected to a pad and a positive line.

Allowable Subject Matter

2. Claims 40-44, 58-59, 63-64 and 67-68 are allowed.

Response to Arguments

3. Applicant argues that since the examiner stated that applicant's arguments with respect to claims 15, 19, 38-39, 45-57, 60-62, 65-66 and 69-72

have been considered but are moot in view of the new grounds of rejection, and since the examiner did not address any of applicant's arguments with respect to claims 15 and 57, applicant assumes that the examiner agrees that the lines connected to the power supply terminals VDD1 and VDD2 can not be read to be the plurality of positive lines required by claims 15 and 57.

The examiner does not agree that the lines connected to the power supply terminals VDD1 and VDD2 can not be read to be the plurality of positive lines required by claims 15 and 57. The examiner still maintains the position that since figure 16 depicts power supply lines 1640-1647, ground line 1610, and I/0 pads 1620 connected in between two diodes, and no pads are connected to the power supply lines and the ground lines, and since the specification does not recite Vcc pads and grounds pads, then the plurality of pads 1620 in figure 16 can only be the I/0 pads which are located in between the two diodes. The examiner stated that applicant's arguments with respect to claims 15, 19, 38-39, 45-57, 60-62, 65-66 and 69-72 have been considered but are moot in view of the new grounds of rejection, because the new rejection does not state that Gen et al. teach a plurality of ESD positive lines not being directly connected to a pad, but rather a plurality of ESD positive lines not being directly connected to said pads. Applicant did not argue that Gen et al. do not teach a plurality of ESD positive lines are not being directly connected to said pads.

4. Applicant does not understand how using two diodes in parallel changes anything, since the inputs of both parallel diodes are still connected to the high

voltage pad VDD1, and the outputs of both parallel diodes are still connected to bus R1.

Connecting a pair of additional parallel head to tail diodes between each high voltage supply (VDD) and the bus (R1), next to the high voltage supply (VDD), means that the plurality of ESD positive lines are not directly connected to the VDD pads, because these additional diodes are located between the plurality of ESD positive lines and the VDD pads.

5. Applicant argues that the examiner did not state why one skilled in the art would be motivated to modify Gen et al.'s circuit, and thus did not set forth a prima facia case of obviousness.

The examiner stated that it would also have been obvious to a person of ordinary skill in the art at the time the invention was made to connect a pair of parallel head to tail diodes between each high voltage supply (VDD) and the bus (R1) in Gens et al.'s device, in order to improve the isolation between the various power supply sources.

6. Applicant argues that the change suggested by the examiner would no longer allow a diode D2, or the entire circuit, or operate as intended.

The examiner does not understand why the changes thereof would no longer allow diode D2, or the entire circuit, to operate as intended.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
August 30, 2004

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800